DATA SHEET

PCB2421
1K dual mode serial EEPROM

Preliminary specification
Supersedes data of 1995 Oct 11
File under Integrated Circuits, IC12

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Philips
Semiconductors

PHILIPS

CONTENTS

1K dual mode serial EEPROM PCB2421

1 FEATURES

- Single supply with operation 4.5 to 5.5 V
- Completely implements DDC1/DDC2B interface for monitor identification
- Low power CMOS technology
- Two-wire I^2C-bus interface
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- Write-protect pin
- 100 kHz I^2C-bus compatibility
- Designed for 10000 erase/write cycles minimum
- Data retention greater than 10 years
- 8-pin DIP and SO package
- Temperature range 0 to +70 °C.

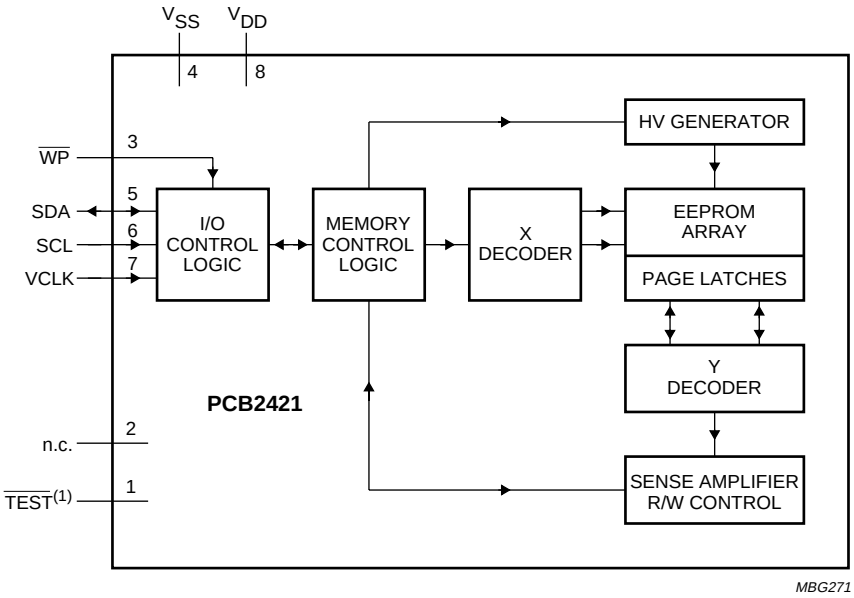
2 GENERAL DESCRIPTION

The Philips PCB2421 is a 128 × 8-bit dual mode serial Electrically Erasable PROM (EEPROM).
This device is designed for use in applications requiring storage and serial transmission of configuration and control information. Two modes of operation have been implemented: transmit-only mode (DDC1 mode) and bidirectional mode (DDC2B, or I^2C-bus mode). Upon power-up, the device will be in the transmit-only mode, sending a serial bitstream of the entire memory array contents, clocked by the VCLK pin. A valid HIGH-to-LOW transition on the SCL pin will cause the device to enter the bidirectional mode, with byte selectable read/write capability of the memory array. The PCB2421 is available in a standard 8-pin dual in-line and 8-pin small outline package operating in a commercial temperature range.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCB2421P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCB2421T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4 BLOCK DIAGRAM



(1) Factory use only.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{TEST}$	1	factory use only: must be tied to V_{DD}; may not be left open-circuit
n.c.	2	may be tied to V_{SS}, V_{DD}, or left open-circuit
$\overline{WP}$	3	write protect input (LOW = write protected, HIGH = not write protected); may not be left open-circuit
V_{SS}	4	ground
SDA	5	serial data input/output
SCL	6	serial clock input/output (DDC2B)
VCLK	7	serial clock input (transmit-only mode, DDC1)
V_{DD}	8	supply voltage

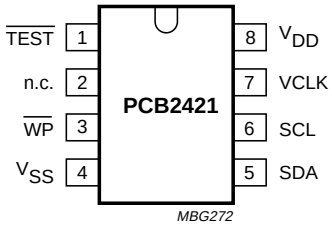


Fig.2 Pin configuration.

6 FUNCTIONAL DESCRIPTION

The PCB2421 operates in two modes, the transmit-only mode (DDC1) and the bidirectional mode (DDC2, or I^2C-bus mode). There is a separate two-wire protocol to support each mode, each having a separate clock input and sharing a common data line (SDA). The device enters the transmit-only mode (DDC1) upon power-up. In this mode the device transmits data bits on the SDA pin in response to a clock signal on the VCLK pin. The device will remain in this mode until a valid HIGH-to-LOW transition is placed on the SCL input. When a valid transition on SCL is recognized, the device will switch into the bidirectional mode (see Fig.3). The only way to switch the device back to the transmit-only mode (DDC1) is to remove power from the device.

6.1 Transmit-only mode (DDC1)

The device will power-up in the transmit-only mode. This mode supports a unidirectional two-wire protocol for transmission of the contents of the memory array (see Fig.12). The PCB2421 requires that it be initialized prior to valid data being sent in the transmit-only mode (see Section “Initialization procedure”, and Fig.4).

In this mode, data is transmitted on the SDA pin in 8-bit bytes, each byte followed by a ninth clock pulse during which time SDA is left high-impedance. The clock source for the transmit-only mode is provided on the VCLK pin; a data bit is output on the rising edge on this pin. The 8 bits in each byte are transmitted most significant bit first. Each byte within the memory array will be output in sequence. When the last byte in the memory array is transmitted, the output will wrap around to the first location and continue. The bidirectional mode clock (SCL) pin must be held HIGH for the device to remain in the transmit-only mode.

6.2 Initialization procedure

At power-on, after V_{DD} has stabilized, the device will be in the transmit-only mode. Nine clock cycles on the VCLK pin must be given to the device for it to perform internal synchronization. During this period, the SDA pin will be in a high-impedance state. On the rising edge of the tenth clock cycle, the device will output the first valid data bit which will be the most significant bit of a byte. The device will power-up with address pointer at 00H (see Fig.4).

6.3 Bidirectional mode (DDC2B, I^2C-bus mode)

The PCB2421 can be switched into the bidirectional mode (see Fig.3) by applying a valid HIGH-to-LOW transition on the bidirectional mode clock (SCL).

When the device has been switched into the bidirectional mode, the VCLK input is disregarded. This mode supports a two-wire bidirectional data transmission protocol (I^2C-bus protocol). In the I^2C-bus protocol, a device that sends data on the bus is defined to be the transmitter, and a device that receives data from the bus is defined to be the receiver. The bus must be controlled by a master device that generates the bidirectional mode clock, controls access to the bus, and generates the START and STOP conditions, while the PCB2421 acts as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

6.3.1 BIDIRECTIONAL MODE BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Fig.6).

6.3.2 BUS NOT BUSY (A)

Both data (SDA) and clock (SCL) lines remain HIGH.

6.3.3 START CONDITION (B)

A HIGH-to-LOW transition of the SDA line while SCL is HIGH determines a START condition. All commands must be preceded by a START condition.

6.3.4 STOP CONDITION (C)

A LOW-to-HIGH transition of the SDA line while SCL is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

6.3.5 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition. The maximum number of data bytes transferred between the START and STOP conditions during a write operation is 8 bytes (see Section “Page write” and Fig.5).

The maximum number of data bytes transferred between START and STOP conditions during a read operation is unlimited.

6.3.6 ACKNOWLEDGE

The PCB2421, when addressed in DDC2B mode, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra (9th) clock pulse which is associated with this acknowledge bit. The PCB2421 does not generate an acknowledge if an internal programming cycle is in progress (SDA line is left HIGH during the 9th clock pulse). The PCB2421 generates an acknowledge by pulling down the SDA line during the acknowledge pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must also be taken into account. The master receiver must signal an end of data to the PCB2421 by **not** generating an acknowledge bit on the last byte that has been clocked out of the slave transmitter. In this case, the slave transmitter PCB2421 must leave the data line HIGH to enable the master to generate the STOP condition.

6.3.7 SLAVE ADDRESS

After generating a START condition, the bus master transmits the slave address (MSB first) consisting of a 7-bit device address (1010000) for the PCB2421. The eighth bit of the slave address determines if the master device wants to read or write to the PCB2421 (R/$\overline{W}$ bit) (see Fig.7). The PCB2421 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Table 1 Slave address

OPERATION	SLAVE ADDRESS	R/$\overline{W}$
Read	1010000	1
Write	1010000	0

6.4 Write operation

6.4.1 BYTE WRITE

Following the START condition from the master, the device address (7 bits), and the R/$\overline{W}$ bit (logic LOW for write) is placed on the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the PCB2421. After receiving another acknowledge signal from the PCB2421, the master device will transmit the data word to be written into the addressed memory location. The PCB2421 acknowledges again and the master generates a STOP condition. This initiates the internal write cycle, and during this time the PCB2421 will not generate acknowledge signals.

6.4.2 PAGE WRITE

For a page write, the write control byte, word address, and the first data byte are transmitted to the PCB2421 in the same way as in a single byte write. But instead of generating a STOP condition the master transmits up to eight data bytes to the PCB2421 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a STOP condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order four bits of the word address remain constant. A maximum of 8 bytes can be written in one operation. As with the byte write operation, once the STOP condition is received an internal write cycle will begin (see Figs 5 and 8).

6.5 Acknowledge polling

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the STOP condition for a write command has been issued from the master, the device initiates the internally timed write cycle. Acknowledge (ACK) polling can be initiated immediately. This involves the master sending a START condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Fig.9 for flow diagram.

6.6 Write protection

Pin 3 is a write protect input ($\overline{WP}$). In the DDC1 mode, the PCB2421 can only be read according to the DDC1 protocol, hence the $\overline{WP}$ input has no effect in this mode. In the DDC2B mode, when $\overline{WP}$ is connected to ground, the entire EEPROM is write-protected, regardless of other pin states. When connected to V_{DD}, write-protection is disabled and the EEPROM may be programmed. $\overline{WP}$ may not be left open-circuit.

Table 2 Mode configurations

DDC	$\overline{WP}$	MODE
DCC1	X[1]	R
DCC2	1	R/W
	0	R

Note

1. Where X = don't care.

6.7 Read operation

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to logic 1. There are three basic types of read operations: current address read, random read, and sequential read.

6.7.1 CURRENT ADDRESS READ

The PCB2421 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address 'n', the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W set to logic 1, the PCB2421 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a STOP condition and the PCB2421 discontinues transmission (see Fig.10).

6.7.2 RANDOM READ

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the PCB2421 as part of a normal write operation. After the word address is sent, the master generates a REPEATED START condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again but with the R/W bit set to logic 1. The PCB2421 will then issue an acknowledge and transmits the 8-bit data word.
The master will not acknowledge the transfer but does generate a STOP condition and the PCB2421 discontinues transmission (see Fig.11).

6.7.3 SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the PCB2421 transmits the first data byte, the master issues an acknowledge as opposed to a STOP condition in a random read.
This directs the PCB2421 to transmit the next sequentially addressed 8-bit word. To provide sequential reads the PCB2421 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

6.8 Pin description

6.8.1 SDA

This pin is used to transfer addresses and data into and out of the device, when the device is in the bidirectional (I^2C-bus, DDC2B) mode. In the transmit-only mode (DDC1), which only allows data to be read from the device, data is also transferred on the SDA pin. This pin is an open-drain terminal, therefore the SDA bus requires a pull-up resistor connected to V_{DD} (typically 10 kΩ for 100 kHz). See brochure *"The I^2C-bus and how to use it"* (order no. 9398 393 40011) or *"Data Handbook IC12"*.

6.8.2 SCL

This pin is the clock input for the bidirectional mode (I^2C-bus, DDC2B), and is used to synchronize data transfer to and from the device. It is also used as the signalling input to switch the device from the transmit-only mode to the bidirectional mode. It must remain HIGH for the chip to continue operation in the transmit-only mode (DDC1).

6.8.3 VCLK

This pin is the clock input for the transmit-only mode (DDC1). In the transmit-only mode, each bit is clocked out on the rising edge of this signal. In DDC2B mode, this input is a don't care.

6.8.4 $\overline{WP}$

This pin is used to inhibit writing of the EEPROM. When this pin is connected to ground, writing of the EEPROM is inhibited. When connected to V_{DD} (and VCLK = V_{DD}), the EEPROM can be programmed. $\overline{WP}$ may not be left open-circuit. $\overline{WP}$ input is a 'don't care' in DDC1 mode.

6.8.5 $\overline{TEST}$

Pins 1 is a $\overline{TEST}$ pin for factory use only. It must be connected to V_{DD} in the application.

6.8.6 N.C.

This pin has no connection and may be tied to V_{SS}, V_{DD} or left open-circuit.

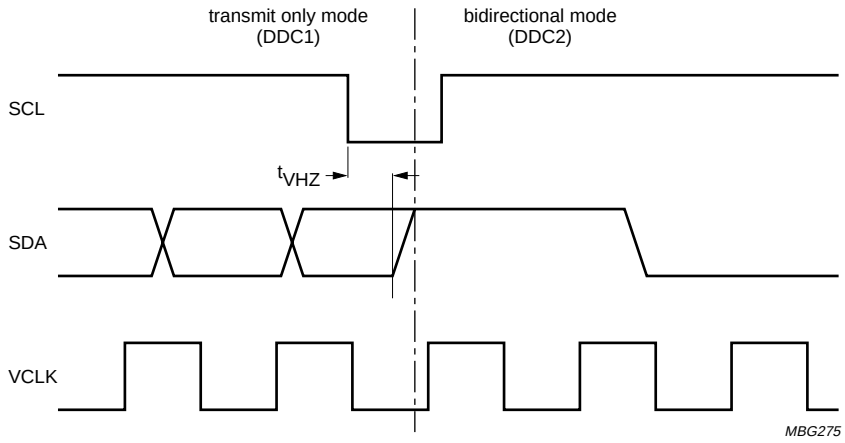


Fig.3 Mode transition diagram.

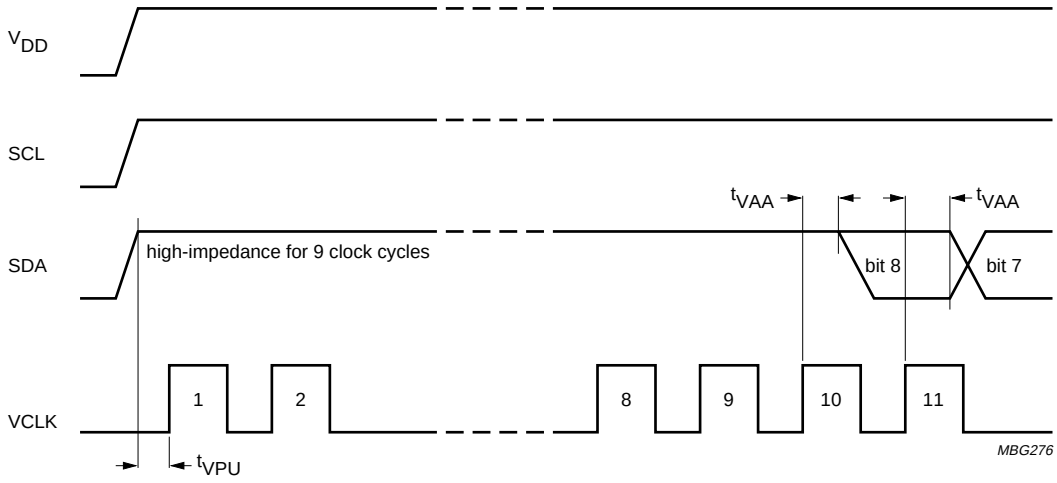
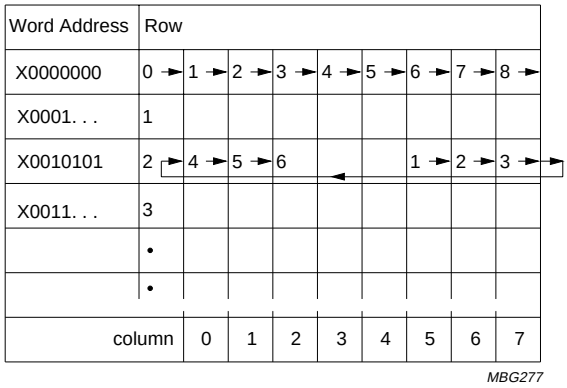


Fig.4 Device initialization diagram.



X = don't care.

Fig.5 Example of writing 8 bytes with word address X0000000 and 6 bytes with word address X0010101.

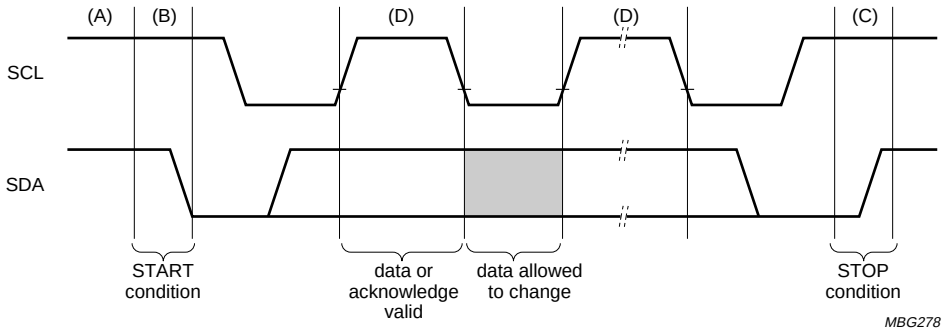


Fig.6 DDC2B data transfer sequence on the I^2C-bus.

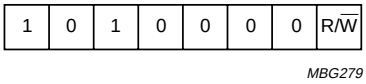


Fig.7 Slave address.

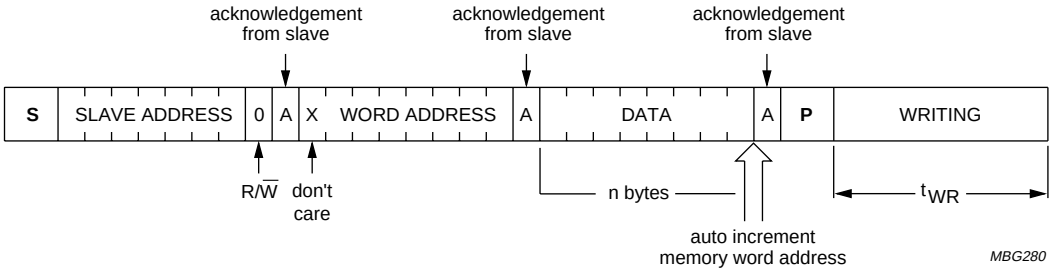


Fig.8 I^2C-bus write protocol (n = maximum 8 bytes).

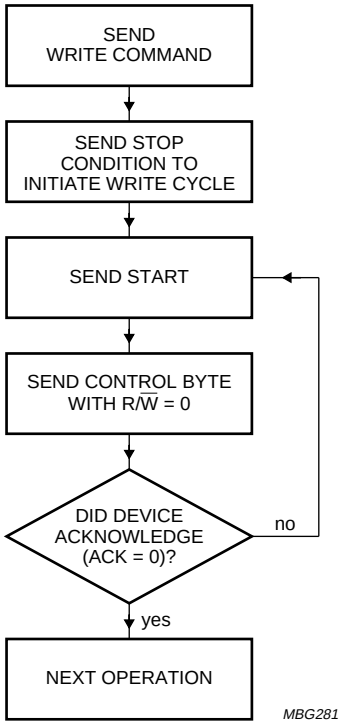


Fig.9 Acknowledge polling.

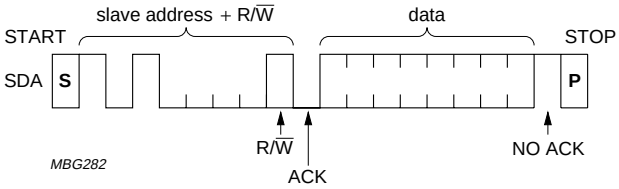


Fig.10 Current address read.

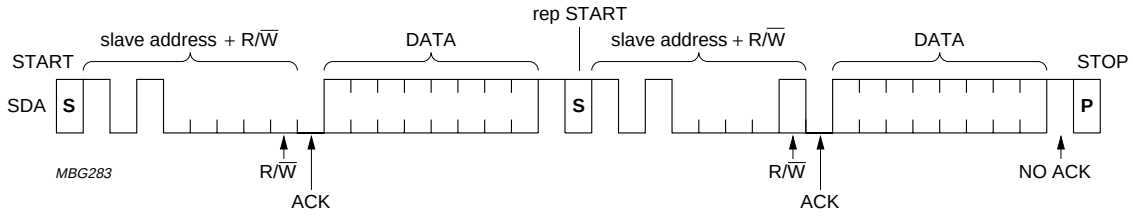


Fig.11 Random read.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.3	+7.0	V
V_n	input voltage on any pin	measured via 500 Ω resistor	–0.5	$V_{DD(max)}$ + 0.5	V
I_I	DC input current		–10	+10	mA
I_O	DC output current		–10	+10	mA
P_{tot}	total power dissipation		–	150	mW
P_o	power dissipation per output		–	50	mW
T_{stg}	storage temperature	without EEPROM retention	–65	+150	°C
		with EEPROM retention	–65	+70	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_{es}	electrostatic discharge	note 1	–2000	+2000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8 DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	–	5.5	V
V_{IH}	HIGH level input voltage (pins 3, 5 and 6)		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage (pins 3, 5 and 6)		–	–	$0.3V_{DD}$	V
$V_{IH(7)}$	HIGH level input voltage (pin 7)		2.0	–	–	V
$V_{IL(7)}$	LOW level input voltage (pin 7)		–	–	0.8	V
V_{OL}	LOW level output voltage	I_{OL} = 3 mA; V_{DD} = 4.5 V	–	–	0.4	V
I_{LI}	input leakage current	V_I = 0 to 5.5 V	–10	–	+10	µA
I_{LO}	output leakage current	V_O = 0 to 5.5 V	–10	–	+10	µA
$I_{DD(write)}$	operating write current	f_{SCL} = 100 kHz; V_{DD} = 5.5 V	–	–	1000	µA
$I_{DD(read)}$	operating read current	f_{SCL} = 100 kHz; V_{DD} = 5.5 V	–	–	400	µA
$I_{DD(st)}$	standby current	V_{DD} = 5.5 V; DDC2B mode; VCLK = SDA = SCL = V_{DD}	–	–	30	µA

9 EEPROM CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WR}	EEPROM write time	–	20	ms
N_{CYC}	EEPROM endurance	10000	–	E/W cycles
t_{RET}	EEPROM retention	10	–	years

10 AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = 0 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DDC1 mode (transmit-only; unidirectional)						
t_{VAA}	output valid from VCLK	see Fig.12; note 1	–	1	–	µs
t_{VHIGH}	VCLK HIGH time	see Fig.12	20	–	–	µs
t_{VLOW}	VCLK LOW time	see Fig.12	20	–	–	µs
t_{VHZ}	mode transition time	see Fig.3; note 1	–	500	–	ns
t_{SP}	input filter spike suppression time		–	–	100	ns
t_{vpu}	DDC1 mode power-up time	see Fig.4	–	5	–	µs
DDC2B mode (bidirectional; I²C-bus mode); see Fig.13						
f_{SCL}	serial clock frequency		0	–	100	kHz
t_{HIGH}	serial clock HIGH time		4	–	–	µs
t_{LOW}	serial clock LOW time		4.7	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{HD;STA}$	START condition hold time		4	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;DAT}$	data input hold time		0	–	–	µs
$t_{SU;DAT}$	data input set-up time		250	–	–	ns
$t_{SU;STO}$	STOP condition set-up time		4	–	–	µs
t_{BUF}	bus free time	note 2	4.7	–	–	µs
t_{SP}	input filter spike suppression		–	–	100	ns

Notes

1. The rise time for SDA returning HIGH must be observed after this period.
2. This is the time that the bus must be free before a new transmission can start.

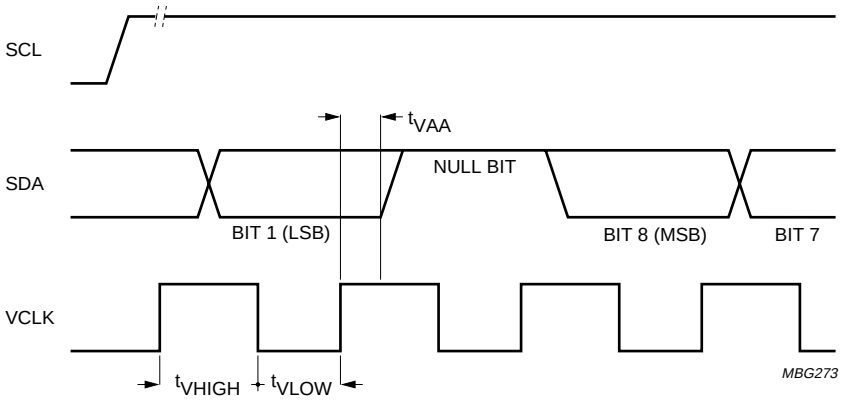


Fig.12 Transmit-only mode (DDC1).

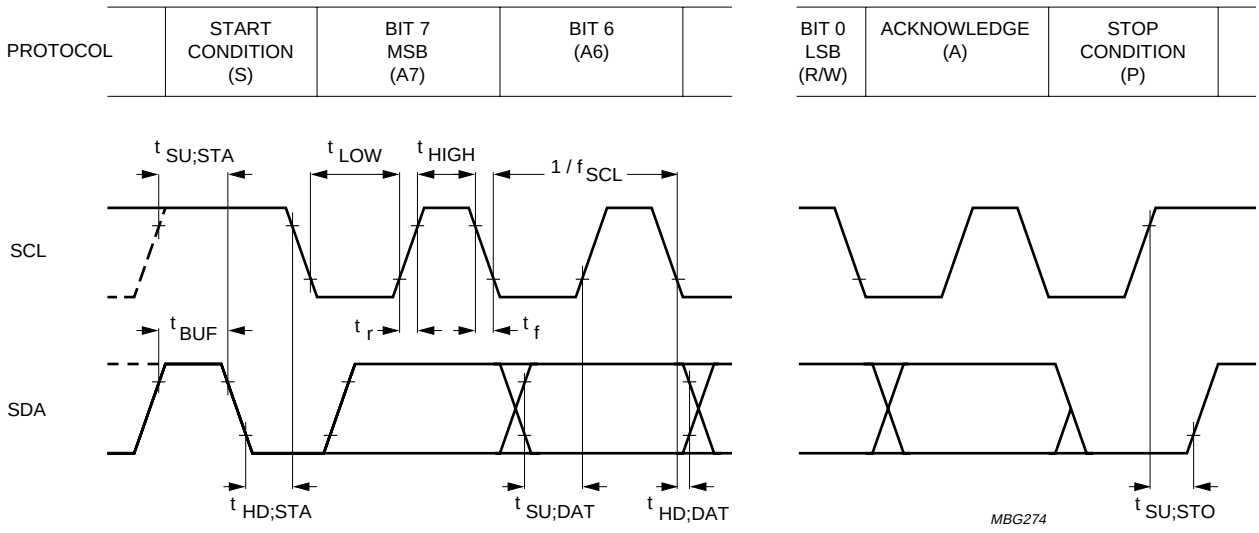


Fig.13 DDC2B (I^2C-bus timing).

11 APPLICATION INFORMATION

11.1 Diode protection

There is no diode connection between VCLK and V_{DD}, SCL and V_{DD} and SDA and V_{DD} (see Fig.14). This allows powering-down the device without affecting the I^2C-bus operation or loading the VCLK driver.

11.2 Functional compatibility with microchip 24CL21 dual mode EEPROM

The Philips PCB2421 is pin and function compatible with the 24CL21 providing the following measures are taken in the application.

1. Pin 1 ($\overline{TEST}$) must be tied to V_{DD}
2. Pin 3 ($\overline{WP}$) must be tied to V_{DD}. This inhibits the write protection function which does not exist on the 24CL21 at this time
3. Maximum 100 kHz DDC2B clock frequency
4. Maximum 25 kHz DDC1 VCLK clock frequency
5. During EEPROM programming a maximum write time of 20 ms must be observed
6. 8-byte maximum during page write must be observed
7. During operation V_{DD} must be between 4.5 and 5.5 V
8. An operating temperature between 0 and +70 °C must be observed
9. Output valid from VCLK (t_{VAA}) typical 1 µs must be observed
10. DDC1 mode power-up time (t_{VPU}) typical 5 µs should be observed.

Remark: VCLK is ‘don’t care’ in the DDC2B mode.

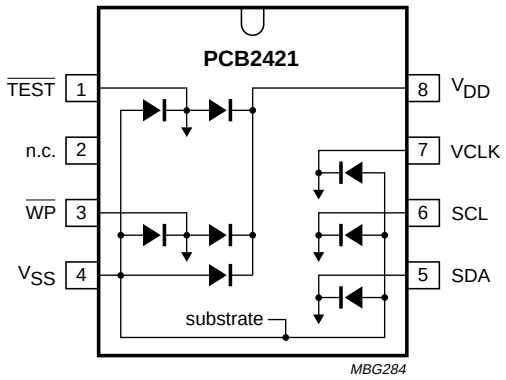
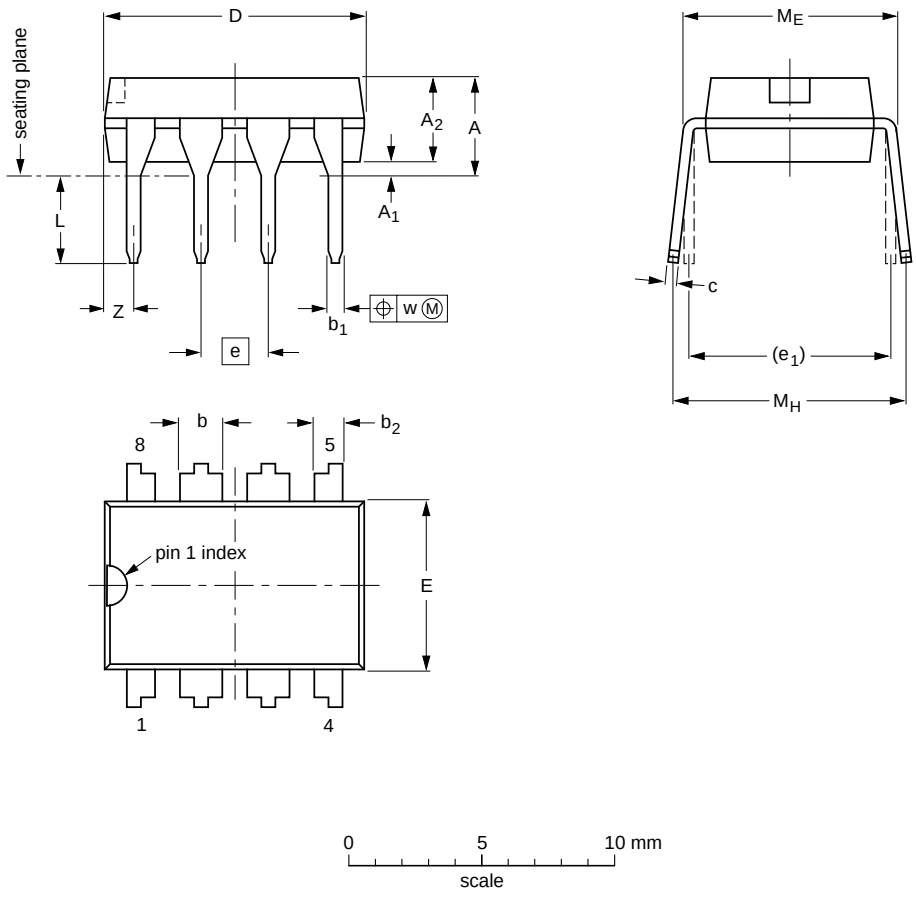


Fig.14 PCB2421 diode protection.

12 PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

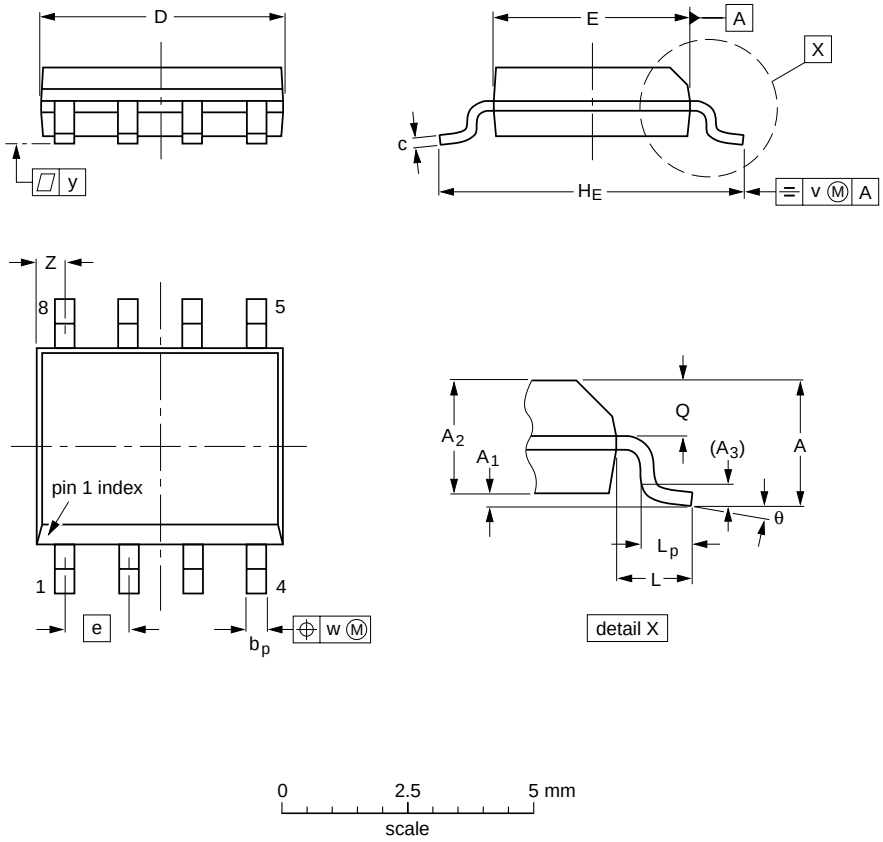
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

13 SOLDERING

13.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

13.2 DIP

13.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

13.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

13.3 SO

13.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

13.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

15 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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